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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/362,504	07/27/1999	KRAMADHATI V. RAVI	AM1126D1/T08	6922
32588	7590	04/21/2004	EXAMINER	
APPLIED MATERIALS, INC. 2881 SCOTT BLVD. M/S 2061 SANTA CLARA, CA 95050			ZERVIGON, RUDY	
			ART UNIT	PAPER NUMBER
			1763	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/362,504

Applicant(s)

RAVI ET AL.

Examiner

Rudy Zervigon

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Jin Onuki et al¹. Onuki teaches an integrated circuit (Figure 4; “LSIs” - Large Scale Interconnections; Abstract, Section 1) formed on a semiconductor substrate (Figure 4; “Si wafers” , Section 2.1) (Figure 4; “Si wafers” , Section 2.1) by the method of:

- a. flowing a process gas (Argon, Section 2.1) into a substrate (Figure 4; “Si wafers” , Section 2.1) processing chamber (inherent, “base pressure before sputtering was 2×10^{-7} Pa” Section 2.1);
- b. forming a plasma (Figure 4, Section 3.1, last paragraph) from said process gas (Argon, Section 2.1) by coupling sputtering energy (“The sputtering power was 4 kW..., Section 2.1, Figure 1a) into said substrate (Figure 4; “Si wafers” , Section 2.1) processing chamber (inherent, “base pressure before sputtering was 2×10^{-7} Pa” Section 2.1)
- c. thereafter, maintaining said plasma (Figure 4, Section 3.1, last paragraph) to deposit a first layer (any one of 18 cycles for depositing “Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1) of a film (“Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1) over said substrate (Figure 4; “Si wafers” , Section 2.1) by sputtering without biasing (Left side - Figure 1a; Section

- 2.1) said plasma (Figure 4, Section 3.1, last paragraph) toward said substrate (Figure 4; “Si wafers” , Section 2.1); and
- d. thereafter, maintaining said plasma (Figure 4, Section 3.1, last paragraph) by maintaining coupling of said sputtering energy (“The sputtering power was 4 kW..., Section 2.1, Figure 1a) into said substrate (Figure 4; “Si wafers” , Section 2.1) processing chamber (inherent, “base pressure before sputtering was 2×10^{-7} Pa” Section 2.1) and biasing (Right side, Figure 1a, Section 2.1) said plasma (Figure 4, Section 3.1, last paragraph) toward said substrate (Figure 4; “Si wafers” , Section 2.1) to deposit a second layer of said film (“Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1) over said first layer (any one of 18 cycles for depositing “Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1), as claimed by claim 16

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 17-19, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) in view of Jin Onuki et al². Boys teaches a sputter coating apparatus (Figure 1; column 4; lines 1-54) including:

¹ High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film* (“Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1)s, Vol. 266 (1995), pp. 182-188.

² High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film* (“Al-0.5wt.%Cu-1wt.%Si films”, Section 2.1)s, Vol. 266 (1995), pp. 182-188.

- i. A substrate (14; Figure 1; column 6, lines 5-40) processing system comprising: a housing (16; Figure 1; column 6, lines 5-40) for forming a vacuum chamber (12; Figure 1; column 6, lines 5-40); a vacuum pump (41; Figure 1; column 8, lines 5-40) for evacuating said vacuum chamber (12; Figure 1; column 6, lines 5-40); a pedestal (14; Figure 1; column 6, lines 5-40 - "mounted by conventional means (not shown)"), located within said housing (16; Figure 1; column 6, lines 5-40), configured to hold a substrate (14; Figure 1; column 6, lines 5-40); a gas distribution system (31-34; Figure 1; column 8, lines 5-40) fluidly coupled to said vacuum chamber (12; Figure 1; column 6, lines 5-40); a plasma (abstract...column 4, lines 3-28) generation system for forming a plasma (abstract...column 4, lines 3-28) from process gas (originating from 31; Figure 1) within said vacuum chamber (12; Figure 1; column 6, lines 5-40) and for selectively biasing (column 7, lines 43-61) said plasma (abstract...column 4, lines 3-28) toward said substrate (14; Figure 1; column 6, lines 5-40); a controller (57,58; Figure 1; column 8, lines 43-54) for controlling said vacuum pump (41; Figure 1; column 8, lines 5-40), said gas distribution system (31-34; Figure 1; column 8, lines 5-40) and said plasma (abstract...column 4, lines 3-28) generation system; a memory (column 8, lines 54-69) coupled to Boy's controller (57,58; Figure 1; column 8, lines 43-54) and storing a program (column 8, lines 54-69) for directing the operation of Boy's system, Boy's program (column 8, lines 54-69) including a set of instructions for depositing a film by first, controlling Boy's gas distribution system (31-34; Figure 1; column 8, lines 5-40) to introduce Boy's process gas (originating from 31; Figure 1) into Boy's chamber (12; Figure 1; column 6, lines 5-40); second, controlling Boy's plasma (abstract...column 4,

- lines 3-28) generation system to form a plasma (abstract...column 4, lines 3-28) from Boy's process gas (originating from 31; Figure 1) by coupling sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and deposit a first layer (column 14, lines 23-35) of Boy's film over Boy's substrate (14; Figure 1; column 6, lines 5-40) – claim 17
- ii. The substrate (14; Figure 1; column 6, lines 5-40) processing system (Figure 1) of claim 19 wherein said source of silicon contains silane, as claimed by claim 31 – Applicant's claim requirement that "said source of silicon contains silane" is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP 2111.02).
- iii. A computer readable storage medium having program (column 8, lines 54-69) code embodied therein, said program (column 8, lines 54-69) code for controlling a substrate (14; Figure 1; column 6, lines 5-29) processing system (Figure 1; column 6, lines 5-29), wherein said substrate (14; Figure 1; column 6, lines 5-29) processing system (Figure 1; column 6, lines 5-29) includes a processing chamber (16; Figure 1; column 6, lines 5-29), a gas delivery system (31-34; Figure 1), a plasma generation system (Figure 1) and a

controller (57,58; Figure 1; column 8, lines 43-54) configured to control the gas delivery system (31-34; Figure 1) and the plasma generation system (Figure 1) said program (column 8, lines 54-69) code controlling the semiconductor processing system (Figure 1; column 8; lines 54-69) to process a wafer in the chamber (16; Figure 1; column 6, lines 5-29) in accordance with the following:

- a. a first set of computer instructions (column 8; lines 54-69) for controlling the gas delivery system (31-34; Figure 1) to introduce a process gas (originating from 31; Figure 1) into the processing chamber (16; Figure 1; column 6, lines 5-29);
- b. a second set of computer instructions (column 8; lines 54-69) for controlling the plasma generation system (62, 63; Figure 1 - column 9; lines 27-46) to form a plasma (column 1, lines 20-40) from the process gas (originating from 31; Figure 1) by coupling sputtering ("sputtering rate and sputtering uniformity"; abstract) energy (column 14, lines 23-30) into said processing chamber (16; Figure 1; column 6, lines 5-29) to deposit a first layer (column 1, lines 42-50) of a film over a substrate (14; Figure 1; column 6, lines 5-29) – claim 32

Boys does not teach:

- iv. by sputtering without biasing Boy's plasma (abstract...column 4, lines 3-28) towards Boy's substrate (14; Figure 1; column 6, lines 5-40); and third, controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and bias Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14;

Figure 1; column 6, lines 5-40) to deposit a second layer of Boy's film over Boy's first layer (column 14, lines 23-35) – claim 17

- v. The substrate (14; Figure 1; column 6, lines 5-40) processing system of claim 17 wherein Boy's program (column 8, lines 54-69) further includes instructions for depositing a plurality of Boy's first layers (column 14, lines 23-35) and Boy's second layers by fourth, depositing a third layer of Boy's film over Boy's second layer by controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and stop biasing (column 7, lines 43-61) Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14; Figure 1; column 6, lines 5-40); fifth, depositing a fourth layer of Boy's film over Boy's third layer by controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and bias Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14; Figure 1; column 6, lines 5-40); and sixth, performing the second and third steps iteratively at least once until a desired thickness of Boy's film is reached – claim 18
- vi. The apparatus of claim 17 wherein said gas distribution system (31-34; Figure 1; column 8, lines 5-40) includes sources of silicon and oxygen fluidly coupled to said gas distribution system (31-34; Figure 1; column 8, lines 5-40), as claimed by claim 19 –
However, it has been held that claim language that simply specifies an intended use or

field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP 2111.02).

- vii. depositing by sputtering (“sputtering rate and sputtering uniformity”; abstract) without biasing (column 7, lines 43-61) Boys’ plasma (column 1, lines 20-40) towards Boys’ substrate (14; Figure 1; column 6, lines 5-29); and
 - a. a third set of computer instructions for controlling Boys’ plasma (column 1, lines 20-40) generation system (31-34; Figure 1) to maintain Boys’ plasma (column 1, lines 20-40) by maintaining coupling of Boys’ sputtering (“sputtering rate and sputtering uniformity”; abstract) energy (column 14, lines 23-30) into Boys’ processing chamber (16; Figure 1; column 6, lines 5-29) and to bias Boys’ plasma (column 1, lines 20-40) toward Boys’ substrate (14; Figure 1; column 6, lines 5-29) to deposit a second layer of Boys’ film over Boys’ first layer (column 1, lines 42-50) – claim 32

Jin Onuki et al is discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Boys to use Jin Onuki’s conventional sputtering method (Fig. 1(a)) as part of Boys’ program

(column 8, lines 54-69) for directing the operation of Boy's system by Boy's controller (57,58; Figure 1; column 8, lines 43-54).

Motivation for Boys to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Boys' program for directing the operation of Boy's system by Boy's controller is to deposit films for conventional "step coverage" and "electromigration resistance" as taught by Jin Onuki (abstract).

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,772,771 A) in view of Jin Onuki et al³. Li et al teaches:

- i. A high-density plasma (column 1, lines 20-40) chemical vapor deposition system (Figure 1; column 3, lines 21-46) comprising:
 - b. a housing (18; Figure 1; column 3, lines 49-65) for forming a vacuum chamber (18; Figure 1; column 3, lines 49-65); a pedestal (14; Figure 1; column 3, lines 49-65), located within said housing (18; Figure 1; column 3, lines 49-65), for holding a substrate (20; Figure 1; column 3, lines 49-65); means for introducing reactants (compare Applicant's 14; Figure 1 to Li's 34; Figure 1) into said vacuum chamber (18; Figure 1; column 3, lines 49-65); means for generating a plasma (compare Applicant's elements 24, 26, and 44; Figure 1 to Li's 25, 8, and 14, respectively; Figure 1) from said reactants by applying a sputtering ("sputtering rate and sputtering uniformity"; abstract) power to said reactants to deposit a first layer (column 1, lines 42-50) of a film on said substrate (20; Figure 1; column 3, lines 49-65) during a first time period said first layer (column 1,

lines 42-50) for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film – claim 20. Applicant's claim requirement of "said first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film" is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP 2111.02).

Li does not teach:

- viii. means for biasing (column 7, lines 43-61) Li's plasma (column 1, lines 20-40) toward Li's substrate (20; Figure 1; column 3, lines 49-65) during a second time period after Li's first time period to enhance a sputtering ("sputtering rate and sputtering uniformity"; abstract) of Li's plasma (column 1, lines 20-40) while maintaining application of Li's sputtering ("sputtering rate and sputtering uniformity"; abstract) power to Li's reactants and deposit Li's subsequent layer

Jin Onuki et al is discussed above.

³ High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-188.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Li to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Li's control for directing the operation of Li's apparatus.

Motivation for Li to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Li's control for directing the operation of Li's apparatus is to deposit films for conventional "step coverage" and "electromigration resistance" as taught by Jin Onuki (abstract).

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,77,2771 A) and Jin Onuki et al⁴ in view of Boys et al (USPat.4,500,408). Li, Shijian et al and Jin et al are discussed above. Li, Shijian et al and Jin et al do not teach:

- ix. The apparatus of claim 20, further comprising means for maintaining a pressure of between about 0.001-10 torr in said vacuum chamber (18; Figure 1; column 3, lines 49-65) while said films are deposited, as claimed by claim 21. Applicant's means for maintaining a pressure is supported in Applicant's page 6 – "A gas distribution system introduces a process gas containing reactants into the vacuum chamber and sets and maintains a selected pressure in the chamber along with a vacuum pump and valve system."
- x. The apparatus of claim 20, further comprising means for maintaining a wafer temperature of between about 100-500°C in said vacuum chamber while said film s are deposited, as claimed by claim 22

Boys et al teach equivalent pressure control means including a gas distribution system (31-34; Figure 1) introduces a process gas (31) containing reactants into the vacuum chamber (16) and

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sets and maintains a selected pressure (column 8; lines 7-13) in the chamber along with a vacuum pump (41) and valve system (32). Boys et al further teaches equivalent temperature control means (claim 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Li, Shijian et al and Jin Onuki et al to add Boys' pressure and temperature control means.

Motivation for Li, Shijian et al and Jin Onuki et al to add Boys' pressure and temperature control means is for controlling the processing during operation as taught by Boys (column 11; lines 14-58).

7. Claims 23, 24, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin Onuki et al⁵ in view of Matsura (USPat. 5,319,247). Jin Onuki teaches:

- i. An integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) formed on a semiconductor substrate (Figure 4; "Si wafers" , Section 2.1), said integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) comprising: (a) a plurality of active devices (LSIs, Section 1) formed in said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); (b) at least one metal layer (Al; Figure 4) formed above said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); and (c) at least one insulating layer (SiO₂; Figure 4) formed between said metal layer (Al; Figure 4) and said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1), said insulating layer (SiO₂; Figure 4) having a plurality of patterned holes (Figure

⁴ High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film* ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s, Vol. 266 (1995), pp. 182-188.

⁵ High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film* ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s, Vol. 266 (1995), pp. 182-188.

- 11) filled with electrically conductive material ("Al"; Figure 4) to electrically connect selected portions of said metal layer (Al; Figure 4) to selected portions of said semiconductor substrate (Figure 4; "Si wafers", Section 2.1) - claim 23
- ii. The integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23, further comprising: (d) a second metal layer ("Al"; Figure 4(3)) formed above said semiconductor substrate (20; Figure 1; column 3, lines 49-65) - claim 24
- iii. The integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23 wherein the first silicon oxide layer (SiO₂; Figure 4) is deposited on the substrate (Figure 4; "Si wafers", Section 2.1) by placing the substrate in a process chamber (inherent, "base pressure before sputtering was 2×10^{-7} Pa" Section 2.1) applying a sputtering power ("The sputtering power was 4 kW...", Section 2.1, Figure 1a) to reactants to generate a plasma in the process chamber - claim 36

Jin Onuki does not teach:

- iv. wherein said insulating layer (SiO₂; Figure 4) comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer – claim 23
- v. Jin Onuki's second metal layer ("Al"; Figure 4(3)) is below said at least one insulating layer (SiO₂; Figure 4); (e) a second insulating layer (SiO₂; Figure 4) formed between said second metal layer ("Al"; Figure 4(3)) and said semiconductor substrate (20; Figure 1; column 3, lines 49-65), said second insulating layer (SiO₂; Figure 4) having a second

plurality of patterned holes (Figure 11) filled with electrically conductive material ("Al"; Figure 4) to electrically connect selected portions of said second metal layer ("Al"; Figure 4(3)) to selected areas of said plurality of active devices (LSIs, Section 1), as claimed by 24

- vi. A second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants, as claimed by claim 36

Matsura teaches a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure: $1\text{mTorr} \leq 100\text{mT} \leq 10\text{Torr}$ (column 6, line 33) and temperature: $100^{\circ}\text{C} \leq 350^{\circ}\text{C} \leq 450^{\circ}\text{C} \leq 500^{\circ}\text{C}$ (column 6, line 38) are specifically met by Matsuura.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform film depositions by sputtering cycles of conventional sputtering (Figure 1(a)) as taught by Jin Onuki thereby depositing plural silicon oxide layers.

Motivation to perform film depositions by sputtering cycles of conventional sputtering (Figure 1(a)) as taught by Jin Onuki thereby depositing plural silicon oxide layers is to deposit films of "superior crack resistance and insulation" as taught by Matsura (silicate, column 6, lines 4-11).

8. Claim 25-30, 33, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) and Jin Onuki et al⁶ in view of Li, Shijian et al (USPat.

⁶ High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film* ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s, Vol. 266 (1995), pp. 182-188.

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5,772,771 A). Boys and Jin Onuki are discussed above. Boys and Jin Onuki do not teach plasma generation by an inductively coupled plasma.

Li teaches inductively coupled plasma generation (8; Figure 1). Li further teaches the inductively coupled plasma (8; Figure 1) is formed from process gas (originating from 70, 72; Figure 1) using only RF energy (10; Figure 1) applied to a coil (8; Figure 1) disposed about the processing chamber (18; Figure 1; column 3, lines 49-65), as claimed by claim 26, 33. Li further teaches the substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 25 wherein said substrate (20; Figure 1; column 3, lines 49-65) processing chamber (18; Figure 1; column 3, lines 49-65) is a high-density plasma (column 1, lines 20-40) chemical vapor deposition chamber (18; Figure 1; column 3, lines 49-65) and said inductively coupled plasma (column 1, lines 20-40) is a high density plasma (column 1, lines 20-40), as claimed by claim 27, 34.

Li further teaches:

- i. The processing system (Figure 1; column 3, lines 21-46) of claim 17 wherein said plasma (column 1, lines 20-40) generating system (Figure 1; column 3, lines 21-46) includes a first electrode (25; Figure 1), a second electrode (14; Figure 1), and a coil (8; Figure 1) disposed about the vacuum chamber (18; Figure 1; column 3, lines 49-65), wherein said pedestal (14; Figure 1; column 3, lines 49-65) includes said second electrode (14; Figure 1), as claimed by claim 30
- ii. The substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 30 wherein the substrate (20; Figure 1; column 3, lines 49-65) is disposed on said second electrode (14; Figure 1) and electric energy (26, 22; Figure 1) is

applied to said first and second electrodes while maintaining the application of said RF energy, as claimed by claim 28

- iii. The substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 17 wherein said process gas (originating from 31; Figure 1) introduced by said gas distribution system (Figure 1; column 3, lines 21-46) (31-34; Figure 1; column 8, lines 5-40) includes flows of silicon and Oxygen, as claimed by claim 29, 35 – Applicant’s claim requirement that the “gas distribution system includes flows of silicon and Oxygen” is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP 2111.02).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Li’s inductively coupled plasma generation (8; Figure 1) to Boys’ and Jin Onuki’s apparatus.

Motivation to add Li’s inductively coupled plasma generation to Boys’ and Jin Onuki’s apparatus is for maintaining high density plasmas as taught by Li (column 1, lines 19-25).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Rudy Zervigon whose telephone number is (571) 272.1442. The examiner can normally be reached on a Monday through Thursday schedule from 8am through 7pm. The official after fax phone number for the 1763 art unit is (703) 872-9306. Any Inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Chemical and Materials Engineering art unit receptionist at (571) 272-1700. If the examiner can not be reached please contact the examiner's supervisor, Gregory L. Mills, at (571) 272-1439.

Rudy Zervigon
4/19/4